

In the Claims

1. (Currently Amended) A method of creating an image, the method comprising:
operating a display to create a linearity error in at least one image bit via a sequence
of bit display periods, said bit display periods comprising:

at least one conflict bit period skewed with respect to other said bit display
periods of the at least one image bit; and

at least two compensating bit periods of the at least one image bit having a bit
period such that the linearity error ~~an uncorrected error~~ created by said skewing occurs during
said compensating bit periods and remains within the image bit. ~~bits, the uncorrected error~~
~~causing an actual weight of at least one image bit to differ from a target weight of that image~~
~~bit.~~

2. (Original) The method of Claim 1 in which said bit period of a first of said at
least two compensating bit periods is shortened and said bit period of a second of said at least
two compensating bit periods is lengthened.

3. (Original) The method of Claim 1 in which said bit period of a first of said at
least two compensating bit periods is lengthened and said bit period of a second of said at
least two compensating bit periods is shortened.

4. (Previously Presented) The method of Claim 1 in which a first and a second
of said at least two compensating bit periods are segments of different image bits.

5. (Original) The method of Claim 1 in which said bit periods of a first and a
second of said at least two compensating bit periods are temporally adjacent said at least one
conflict bit period.

6. (Original) The method of Claim 1 in which said bit periods of a first and a
second of said at least two compensating bit periods are temporally adjacent a combination of
said at least one conflict bit period and at least one other bit period.

7 (Original) The method of Claim 1 in which said bit period of a first of said at least two compensating bit periods occurs prior to said at least one conflict bit period and a second of said at least two compensating bit periods occurs following said at least one conflict bit period.

8. (Original) The method of Claim 7 in which said first compensating bit period corresponds to a first image bit and a second compensating bit period corresponds to a second image bit.

9. (Canceled)

10. (Canceled)

11. (Currently Amended) A display comprising:
an image data source providing a plurality of image data bits; and
a display device comprising at least one display element operable to form an image pixel corresponding to a plurality of image data bits over a sequence of bit display periods, the display periods comprising a linearity error in at least one image bit, said bit display periods comprising:

at least one conflict bit period skewed with respect to other said bit display periods of the at least one image bit; and

at least two compensating bit periods of the at least one image bit having a bit period such that the linearity error ~~an uncorrected error~~ created by said skewing occurs during said compensating bit periods and remains within the image bit. ~~bits, the uncorrected error causing an actual weight of at least one image bit to differ from a target weight of that image bit.~~

12. (Original) The display of Claim 11 in which said bit period of a first of said at least two compensating bit periods is shortened and said bit period of a second of said at least two compensating bit periods is lengthened.

13. (Original) The display of Claim 11 in which said bit period of a first of said at least two compensating bit periods is lengthened and said bit period of a second of said at least two compensating bit periods is shortened.

14. (Previously Presented) The display of Claim 11 in which a first and a second of said at least two compensating bit periods are segments of different image bits.

15. (Original) The display of Claim 11 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent said at least one conflict bit period.

16. (Original) The display of Claim 11 in which said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent a combination of said at least one conflict bit period and at least one other bit period.

17. (Original) The display of Claim 11 in which said bit period of a first of said at least two compensating bit periods occurs prior to said at least one conflict bit period and a second of said at least two compensating bit periods occurs following said at least one conflict bit period.

18. (Original) The display of Claim 17 in which said first compensating bit period corresponds to a first image bit and a second compensating bit period corresponds to a second image bit.

19. (Canceled)

20. (Canceled)

21. (Currently Amended) Logic circuitry for creating an image, the logic circuitry operable when executed to:

operate a display to create a linearity error in at least one image bit via a sequence of bit display periods, said bit display periods comprising:

at least one conflict bit period skewed with respect to other said bit display periods of the at least one image bit; and

at least two compensating bit periods of the at least one image bit having a bit period such that the linearity error ~~an uncorrected error~~ created by said skewing occurs during said compensating bit periods and remains within the image bit. ~~bits, the uncorrected error causing an actual weight of at least one image bit to differ from a target weight of that image bit.~~

22. (Previously presented) The logic circuitry of Claim 21, wherein a first and a second of said at least two compensating bit periods are segments of different image bits.

23. (Previously presented) The logic circuitry of Claim 21, wherein said bit period of a first of said at least two compensating bit periods is shortened and said bit period of a second of said at least two compensating bit periods is lengthened.

24. (Previously presented) The logic circuitry of Claim 21, wherein said bit periods of a first and a second of said at least two compensating bit periods are temporally adjacent a combination of said at least one conflict bit period and at least one other bit period.